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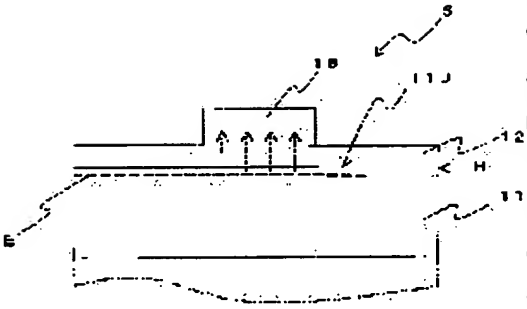
(54) SEMICONDUCTOR DEVICE



(57)Abstract:
PROBLEM TO BE SOLVED: To provide various types of high performance semiconductor devices such as a field-effect transistor which can operate at high frequency, with high output and high efficiency by realizing a stable, low resistance ohmic contact.
SOLUTION: This semiconductor device comprises a first nitride semiconductor layer (11), a second nitride semiconductor layer (12) which is formed on the first layer and has a larger band gap than that of the first layer, and an electrode (18) formed on the second layer. The second nitride semiconductor layer has lattice distortion caused by the difference in lattice constants between the first layer and the second layer, and by tunneling electrons accumulated in the vicinity of the heterointerface (H) of the first nitride semiconductor layer into the n-side electrode, the contact resistance of the n-side electrode can be reduced.

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CLAIMS

[Claim(s)]

[Claim 1] The 1st nitride semi-conductor layer and the 2nd nitride semi-conductor layer which is prepared on said 1st nitride semi-conductor layer, and has a bigger band gap than said 1st nitride semi-conductor layer, It has the electrode prepared on said 2nd nitride semi-conductor layer. Said 2nd nitride semi-conductor layer The semiconductor device characterized by reducing contact resistance of said electrode by making said electrode tunnel the electron which has a lattice strain resulting from a difference of the lattice constant between said 1st nitride semi-conductor layer, and was accumulated near the hetero interface of said 1st nitride semi-conductor layer.

[Claim 2] It is prepared on the 1st [with wurtzite type structure] nitride semi-conductor layer, and said 1st nitride semi-conductor layer. The 2nd nitride semi-conductor layer which said the 1st nitride semi-conductor layer and lattice constant differ from each other, and has a bigger band gap, and has not carried out grid relaxation, It has the electrode prepared on said 2nd nitride semi-conductor layer. The thickness of said 2nd nitride semi-conductor layer The semiconductor device characterized by considering as the range which the fall of contact resistance of said n lateral electrode by the tunnel current component to said electrode of the electron accumulated near the hetero interface of said 1st nitride semi-conductor layer produces.

[Claim 3] It is prepared on the 1st [with wurtzite type structure] nitride semi-conductor layer, and said 1st nitride semi-conductor layer. said the 1st nitride semi-conductor layer and lattice constant -- different -- it having 7s persons and a bigger band gap, and with the 2nd nitride semi-conductor layer which has not carried out grid relaxation The source electrode and drain electrode which were prepared on said 2nd nitride semi-conductor layer, It has the shot key gate electrode prepared on said 2nd nitride semi-conductor layer. The thickness of said 2nd nitride semi-conductor layer The semiconductor device characterized by considering as the range which the fall of contact resistance of said source electrode by the tunnel current component to said source electrode and drain electrode of the electron

accumulated near the hetero interface of said 1st nitride semi-conductor layer and a drain electrode produces.

[Claim 4] It is alternatively prepared on the 1st [with wurtzite type structure] nitride semi-conductor layer, and said 1st nitride semi-conductor layer. The 2nd nitride semi-conductor layer which said the 1st nitride semi-conductor layer and lattice constant differ from each other, and has a bigger band gap, and has not carried out grid relaxation, The 3rd nitride semi-conductor layer which is alternatively prepared on said 1st nitride semi-conductor layer, and has a bigger band gap than said 1st nitride semi-conductor layer, The source electrode and drain electrode which were prepared on said 2nd nitride semi-conductor layer, It has the shot key gate electrode prepared on said 3rd nitride semi-conductor layer. The thickness of said 2nd nitride semi-conductor layer The semiconductor device characterized by considering as the range which the fall of contact resistance of said source electrode by the tunnel current component to said source electrode and drain electrode of the electron accumulated near the hetero interface of said 1st nitride semi-conductor layer and a drain electrode produces.

[Claim 5] The thickness of said 2nd nitride semi-conductor layer is the semiconductor device of claim 1-4 characterized by being 6nm or less given in any one.

[Claim 6] The front face of said nitride semi-conductor layer of 1 where the laminating of said 2nd nitride semi-conductor layer is carried out is the semiconductor device of any one publication of claim 1-5 characterized by being an III group element side.

[Claim 7] It is the semiconductor device of any one publication of claim 1-6 characterized by for said 1st nitride semi-conductor layer consisting of GaN, and said 2nd nitride semi-conductor layer consisting of AlGaN.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[Field of the Invention] It is efficient and especially this invention relates to high power, a RF, and the semiconductor device that operates, when it is a semiconductor device using a nitride semi-conductor, and the ohmic contact to an electron is formed certainly, for example, is applied to a transistor about a semiconductor device.

[Description of the Prior Art] GaN which is a nitride semi-conductor has wide forbidden-band width of face, and it is easy to form a heterojunction with AlGaN, and it is, being applied to various kinds of optical devices and electron devices, since the

property is extensively controllable by adjusting aluminum presentation ratio. For example, MESFET using a nitride semi-conductor (Metal-Semiconductor Field Effect Transistor) Actuation by the high voltage is possible for field-effect transistors, such as HEMT (High Electron Mobility Transistor) or MODFET (Modulation-Doped FET), and they are expected as a power component of high power. In the case of HEMT structure, there is an advantage which can accumulate a more high-concentration two-dimensional electron in a hetero interface compared with the GaAs system HEMT, and it is supposed especially that it is promising. Drawing 11 is a mimetic diagram showing the important section cross-section structure of the conventional GaN system HEMT. That is, as expressed to this drawing, in the conventional HEMT, the layer structure which formed the wurtzite type structure GaN layer 111 used as a channel layer on silicon on sapphire or a SiC substrate (not shown), and formed the AlxGa(1-x) N (0< x<1) layer 112 with a thickness of 20nm - 30nm it is thin to desired threshold voltage on this layer 111 is used. And the shot key gate 120, the source electrode 118, and the drain electrode 119 are formed on this AlxGa(1-x) N layer 112. [Problem(s) to be Solved by the Invention] By the way, one of high power, efficient, and the important technical problems for carrying out high frequency operation is fully reducing contact resistivity [in / for such a transistor / a source drain electrode]. If resistivity is large, parasitism resistance will increase, and the knee voltage in a drain current characteristic will become high, and a transconductance will become low. As the result, the problem that output power, power load effectiveness, and clock frequency fall arises. As ohmic contact to the field-effect transistor using a nitride semi-conductor, comparatively good ohmic contact is acquired in the laminated structure of (Titanium Ti) / aluminum (aluminum). However, the property was sharply changed by the thickness ratio of titanium and aluminum, annealing temperature, and time amount (206 **** technique besides Kasahara, ED99- 1999), and finding out good conditions had the problem of being very difficult. The same problem is similarly produced in various kinds of semiconductor devices using nitride semi-conductors not only including a transistor but a light emitting device. That is, also in semiconductor devices, such as LED and semiconductor laser, the contact resistance between a nitride semi-conductor and an electrode serves as a key which determines various kinds of important properties, such as luminescence reinforcement and the temperature characteristic. Therefore, to realize good ohmic contact is strongly desired over the semiconductor device at large which used the nitride semi-conductor. This invention is made based on recognition of this technical problem. That is, the purpose realizes ohmic contact of low resistance to stability, and it is

efficient and it is to offer various kinds of semiconductor devices of high performance including high frequency, high power, and the field-effect transistor that operates.
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the 1st semiconductor device of this invention The 1st nitride semi-conductor layer and the 2nd nitride semi-conductor layer which is prepared on said 1st nitride semi-conductor layer, and has a bigger band gap than said 1st nitride semi-conductor layer, It has the electrode prepared on said 2nd nitride semi-conductor layer. Said 2nd nitride semi-conductor layer It is characterized by reducing contact resistance of said n lateral electrode by making said electrode tunnel the electron which has a lattice strain resulting from a difference of the lattice constant between said 1st nitride semi-conductor layer, and was accumulated near the hetero interface of said 1st nitride semi-conductor layer. According to the above-mentioned configuration, decline in the contact resistivity by making an electrode tunnel the electron accumulated in the hetero interface is obtained, and the various properties of a semiconductor device can be raised. On the other hand, the 2nd semiconductor device of this invention has wurtzite type structure. The 1st nitride semi-conductor layer, The 2nd nitride semi-conductor layer which it is prepared on said 1st nitride semi-conductor layer, and said the 1st nitride semi-conductor layer and lattice constant differ from each other, and has a bigger band gap, and has not carried out grid relaxation, It has n lateral electrode prepared on said 2nd nitride semi-conductor layer. The thickness of said 2nd nitride semi-conductor layer It is characterized by considering as the range which the fall of contact resistance of said electrode by the tunnel current component to said n lateral electrode of the electron accumulated near the hetero interface of said 1st nitride semi-conductor layer produces. Also by the above-mentioned configuration, decline in the contact resistivity by making an electrode tunnel the electron accumulated in the hetero interface is obtained, and the various properties of a semiconductor device can be raised. Moreover, the 1st [with wurtzite type structure in the 3rd semiconductor device of this invention] nitride semi-conductor layer, The 2nd nitride semi-conductor layer which it is prepared on said 1st nitride semi-conductor layer, and said the 1st nitride semi-conductor layer and lattice constant differ from each other, and has a bigger band gap, and has not carried out grid relaxation, The source electrode and drain electrode which were prepared on said 2nd nitride semi-conductor layer, It has the shot key gate electrode prepared on said 2nd nitride semi-conductor layer. The thickness of said 2nd nitride semi-conductor layer It is characterized by considering as the range which the fall of contact resistance of said source electrode by the tunnel current component to said

source electrode and drain electrode of the electron accumulated near the hetero interface of said 1st nitride semi-conductor layer and a drain electrode produces. According to the above-mentioned configuration, decline in the contact resistivity of the source electrode by making an electrode tunnel the electron accumulated in the hetero interface and a drain electrode is obtained, and the various properties of a semiconductor device can be raised. Moreover, the 1st [with wurtzite type structure in the 4th semiconductor device of this invention] nitride semi-conductor layer, The 2nd nitride semi-conductor layer which it is alternatively prepared on said 1st nitride semi-conductor layer, and said the 1st nitride semi-conductor layer and lattice constant differ from each other, and has a bigger band gap, and has not carried out grid relaxation, The 3rd nitride semi-conductor layer which it is alternatively prepared on said 1st nitride semi-conductor layer, and said the 1st nitride semi-conductor layer and lattice constant differ from each other, and has a bigger band gap, The source electrode and drain electrode which were prepared on said 2nd nitride semi-conductor layer, It has the shot key gate electrode prepared on said 3rd nitride semi-conductor layer. The thickness of said 2nd nitride semi-conductor layer It is characterized by considering as the range which the fall of contact resistance of said source electrode by the tunnel current component to said source electrode and drain electrode of the electron accumulated near the hetero interface of said 1st nitride semi-conductor layer and a drain electrode produces. Also by the above-mentioned configuration, decline in the contact resistivity of the source electrode by making an electrode tunnel the electron accumulated in the hetero interface and a drain electrode is obtained, and the various properties of a semiconductor device can be raised. Here, in the above 1st thru/or the 4th semiconductor device, the thickness of said 2nd nitride semi-conductor layer makes the thing which is 6nm or less, then a tunnel current component increase notably, and it becomes possible to reduce contact resistance of it sharply. Moreover, the front face of said nitride semi-conductor layer of 1 where the laminating of said 2nd nitride semi-conductor layer is carried out can acquire notably the effectiveness of the charge storage by the thing which is an III group element side, then polarization. Said 1st nitride semi-conductor layer consists of GaN, said 2nd nitride semi-conductor layer is easy to apply for the thing which consists of AlGaN, then many semiconductor devices, and, moreover, the effectiveness of reduction of contact resistance is acquired certainly. For example, if this invention is applied to a transistor, between the metals used as the two-dimensional electron accumulated in the hetero interface, and an ohmic electrode, the current by tunneling is increased and the ohmic electrode of low

resistivity can be obtained. Consequently, it becomes possible to operate a field-effect transistor by high power, efficient, and the RF. in addition, this application specification -- setting -- "a nitride semi-conductor" -- B1-x-y-zInxAlyGazN (x<=1, y<=1, z<=1, x+y+z<=1) -- the semi-conductor of all presentations to which the presentation ratio x, and y and z were changed by each within the limits in the chemical formula shall be included Furthermore, what introduced various kinds of impurities, such as predetermined n mold or predetermined p mold dopant, and a proton, oxygen (O), iron (Fe), into these shall be contained in a "nitride semi-conductor."

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail, referring to a drawing. Drawing 1 is a mimetic diagram showing the important section cross-section structure of the semiconductor device of this invention. That is, this drawing is a conceptual diagram which carried out the enlarged display of the cross-section structure of the part of the electrode of a semiconductor device S. As such a semiconductor device, light emitting diodes including the transistor behind raised as an example, semiconductor laser, or various kinds of optical devices and electron devices in addition to this can be mentioned. These semiconductor devices may be formed on substrates, such as sapphire and SiC, and may not have such a substrate. And according to this invention, in the formation section of the electrode of these semiconductor devices S, it has the structure by which the laminating was carried out to the 1st nitride semi-conductor layer 11, the 2nd nitride semi-conductor layer 12, an electrode 18, and the order of ****. Hereafter, these components are explained in detail. First, the 1st nitride semi-conductor layer 11 has wurtzite type structure, is in the condition, i.e., the condition that it has an original lattice constant in a free condition as it is, that the crystal lattice is not substantially distorted with external stress etc., and is prepared in some bodies [at least] of the semiconductor device which is not illustrated. As an example of the 1st nitride semi-conductor layer 11, GaN can be mentioned, for example. Moreover, III group elements other than Ga could be added by GaN besides GaN. Furthermore, top-face 11U of this 1st nitride semi-conductor layer is a field (0001), and it is desirable that it is an III group element side. For example, when this layer 11 consists of GaN, as for that top-face 11U, it is desirable that it is a gallium (0001) (Ga) side. Next, the 1st nitride semi-conductor layer 11 and lattice constant differ from each other, and the 2nd nitride semi-conductor layer 12 has a bigger band gap, and has not carried out grid relaxation. That is, the 2nd nitride semi-conductor layer 12 is made into the condition that the crystal lattice was distorted in response to external stress.

Typically as a factor which produces this "distortion", the difference in a lattice constant with the 1st nitride semi-conductor layer can be mentioned. That is, misfit distortion can be introduced into the 2nd nitride semi-conductor layer 12 by carrying out the laminating of the 2nd nitride semi-conductor layer 12 on the 1st nitride semi-conductor layer 11 from which a lattice constant differs. As an example of the 2nd nitride semi-conductor layer 12, AlGaN can be mentioned, for example. that is, swerve on the 1st nitride semi-conductor layer 11 which consists of GaN etc. -- where grid relaxation is carried out, the laminating of the AlGaN with a large ** band gap is carried out. Furthermore, it is desirable that it is thinner than the predetermined range, and, as for the 2nd nitride, the thickness has the range of thickness where the tunnel current component more specifically turned to the electrode 18 from the 1st nitride semi-conductor layer 11 is obtained substantially, as for a layer 12. As for the thickness, typically, it is desirable to be referred to as 6nm or less. The electrode 18 is formed on such 2nd nitride semi-conductor layer 12. As an electrode 18, a thing well-known as an ohmic electrode material of the nitride semi-conductor of n mold can be used suitably. For example, the structure where the laminating of titanium (Ti) and the aluminum (aluminum) was carried out to this order can be used. According to the structure explained above, the contact resistance by the side of n of a semiconductor device S is reduced, and good ohmic contact is obtained. Hereafter, the reason is explained in full detail. For example, in the structure which carried out the laminating of the AlxGa(1-x) N layer on GaN, when an AlxGa(1-x) N layer does not carry out grid relaxation, it is known that the charge by big piezo polarization and spontaneous polarization will be generated (J.Appl.Phys[besides Ambacher]., 85.no.6, p.3222, 1999). The 1st nitride semi-conductor layer 11 in the condition that it has an original lattice constant in the free condition of wurtzite type structure as it is If the laminating of the 2nd nitride semi-conductor layer 12 (for example, AlxGa(1-x) N) which does not carry out grid relaxation is carried out to Ga side of (GaN [for example,]) The positive charge by piezo polarization and spontaneous polarization is accumulated in that hetero interface H, and the electron E which balanced this charge at coincidence is accumulated into the 1st [near the hetero interface H] nitride semi-conductor layer 11. With the structure of this invention, by making thin thickness of the 2nd nitride semi-conductor layer 12 (for example, AlxGa(1-x) N) which carries out a laminating on the 1st nitride semi-conductor layer 11 (for example, GaN), the distance of the hetero interface H and an electrode 18 becomes short, and it is made easy that the electron E accumulated in the hetero interface H flows into an electrode 18. When AlGaN is used as 2nd nitride semi-conductor layer 12 depending

on the positive charge by piezo polarization and spontaneous polarization which are generated in an interface, it depends for the electron density of the hetero interface H to the mole ratio of aluminum (aluminum) strongly. A phenomenon which was explained above is not looked at by the heterojunction of a GaAs system, but is a phenomenon peculiar to terrorism junction in that of a nitride semi-conductor system. Drawing 2 is a graphical representation showing the potential distribution of the conduction band lower part in the structure which formed aluminum0.3Ga0.7N on GaN and carried out the laminating of the titanium (Ti) on aluminum0.3Ga0.7N further. That is, this graph is the result of solving Poisson's equation and being obtained by count. Moreover, aluminum0.3Ga0.7N presupposed that the Donna concentration is n mold of 1x1018cm-3 here. Moreover, it was presupposed that there is a charge by piezo polarization and spontaneous polarization corresponding to this junction in the interface of aluminum0.3Ga0.7N and GaN. Furthermore, in this count, thickness d of aluminum0.3Ga0.7N was changed with 2nm, 10nm, and 20nm, and the electron presupposed that Fermi-Dirac's distribution is followed. As expressed to drawing 2 , also in which structure, potential well W is formed near the hetero interface. And an electron is accumulated in the part of these potential well W. It turns out that aluminum0.3Ga0.7N was made thin, potential well W has done thickness also as only 2nm, and an electron is accumulated in a hetero interface. in order for the electron accumulated in this part to flow by tunneling to the metal electrode 18 on the front face of a semi-conductor -- aluminum0.3Ga0.7N -- thin -- carrying out -- a potential barrier -- it is effective to make it thin and it can be expected by doing in this way that a current will increase. From the potential distribution illustrated to drawing 2 to drawing 1 The balance of the thermionic-emission current and tunnel current which are taken out by the electrode 18 in ****** is calculable. Drawing 3 is a graphical representation showing the rate to the thermionic emission current of the tunnel current in the structure of drawing 1 . That is, the axis of abscissa of this drawing expresses the thickness of aluminum0.3Ga0.7N (2nd nitride semi-conductor layer 12), and an axis of ordinate expresses the rate to the thermionic emission current of the tunnel current which escapes from this semi-conductor layer and flows. Moreover, carrier concentration of aluminum0.3Ga0.7N was made into 3 level of 1x1018cm-3, 1x1019cm-3, and 5x1019cm-3 here. which [drawing 3 to] carrier concentration -- also setting -- aluminum0.3Ga0.7N layer thickness -- if it becomes thin, the inclination for the rate of tunnel current to increase will be seen. When the carrier concentration of aluminum0.3Ga0.7N is 1x1018cm-3, it turns out that a tunnel current component will begin to increase if thickness becomes thinner than about 20nm, and it

will increase rapidly if thickness becomes thinner than about 10nm. Moreover, when carrier concentration is 1x1019cm-3, if thickness becomes thinner than about 15nm, a tunnel current component will begin to increase, and if thickness becomes thinner than about 8nm, it will increase rapidly. On the other hand, when carrier concentration is 5x1019cm-3, if thickness becomes thinner than about 8nm, a tunnel current component will begin to increase, and if thickness becomes thinner than about 6nm, it will increase rapidly. Thus, when it becomes thinner than criticality--respectively thickness, the fall of the contact resistance by tunnel current will be obtained notably. From the data of tunnel current which was illustrated to drawing 3 , and a thermionic-emission current, the contact resistivity of an electrode 18 is calculable. Drawing 4 is a graphical representation showing the contact resistivity of the electrode 18 in the structure of drawing 1 . When the Donna concentration is 1x1018cm-3, for example and the thickness which is aluminum0.3Ga0.7N is set to 10nm or less from this drawing, it turns out that contact resistivity falls rapidly. Moreover, even if it sees the data of other concentration level, it turns out that contact resistivity will fall clearly if the thickness of aluminum0.3Ga0.7N is set to 10nm or less, and it will fall notably if set to 6nm or less. Although change of resistance was expressed to drawing 4 about the Donna concentration of 3 level here, respectively, if thickness is made thin to 2nm, resistivity will be converged on one point, without being hardly dependent on the Donna concentration. Using effective-mass approximation of a semi-conductor, the result expressed to drawing 4 shows that resistivity can be reduced, so that the 2nd nitride semi-conductor layer (for example, AlGaN) is thin. In fact, the thickness of the 2nd nitride semi-conductor layer (for example, aluminum0.3Ga0.7N) needs to be larger than a lattice constant at least. If process fluctuation is considered, the thickness of the 2nd nitride semi-conductor layer 12 needs to be twice [more than] the lattice constant of a c-axis, and when AlxGa(1-x) N is used, the thickness needs to be 1.2nm or more which hits twice with a lattice constant of 0.6nm. By the way, as for contact resistivity, according to the result expressed to drawing 4 , the thickness of aluminum0.3Ga0.7N will become that the Donna concentration is the order of 1018cm-3 with two or more 0.1-ohmcm and a very high value by 20nm - 30nm like the conventional transistor structure. However, it is in performing RIE (Reactive Ion Etching) processing before vacuum evaporationo of an ohmic electrode in an actual process ****. Since 600 degrees C - 900 degrees C elevated-temperature annealing is performed after electrode vacuum evaporationo, it is expected that the effectual carrier concentration on the front face of a semi-conductor is increasing. If GaN is annealed at 850 degrees

C according to Schloss and others, it is reported that carrier concentration rises a single figure (Appl.Phya.Lett., 68, No.19, p.2702, 1996). On the other hand, in the case of the usual GaN system HEMT, it is the Donna concentration of AlxGa(1-x) N so that a shot key property may not deteriorate but a two-dimensional electron may moreover be accumulated in high concentration x(1-5)1018cm-3 It carries out in many cases. If Schloss's and others report is followed, to set effectual carrier concentration to x(1-5)1019cm-3 will be considered by A 2-RU at the time of ohmic electrode formation. Therefore, when applying this invention to such a transistor, in order to acquire the effectiveness of resistivity reduction according [carrier concentration] to the lamination of AlxGa(1-x) N also in 5x1019cm-3, it is more desirable [the thickness of AlxGa(1-x) N] than the result of drawing 4 to be referred to as 6nm or less.

[Example] Hereafter, the gestalt of operation of this invention is further explained to a detail, referring to an example.

(The 1st example) Drawing 5 is a mimetic diagram showing the important section cross-section structure of the heterojunction field-effect transistor as the 1st example of this invention. Namely, on the GaN channel layer 11, the laminating of the thickness is carried out and, as for this transistor, the 1nm or more AlxGa(1-x) N layer 12 6nm or less has [the source electrode 18, the drain electrode 19 and the gate electrode 20] on this the structure formed, respectively. The structure of this field-effect transistor is explained hereafter, referring to that production process. First, on the silicon on sapphire (0001) which is not illustrated or a SiC substrate, it is thin, for example, about 4nm of nucleation layers which consist of AlN is formed. besides -- the GaN layer 11 of undoping -- MOCVD (Metal-Organic Chemical Vapor Deposition: organic metal chemical vapor deposition) -- it is fully thick, for example, is made to grow up to be the thickness of 2 micrometers by law next, the aluminum0.3Ga0.7N layer from which the mole ratio x of aluminum is set to 0.3 as an AlxGa(1-x) N (0< x<1) layer 12 -- the thickness of the range of 1nm - 6nm, for example, the thickness of 2nm, -- the same -- MOCVD -- it forms by law. The 1st material gas of the organometallic compound (for example, trimethylgallium) containing Ga, the 2nd material gas of the organometallic compound (for example, trimethylaluminum) containing aluminum, and the 3rd material gas (for example, ammonia) containing nitrogen can be used for the crystal growth by these MOCVD(s). Although aluminum0.3Ga0.7N layer 12 was good also as an n mold also as undoping, it was taken as the layer which contains silicon (Si) as an impurity so that the Donna concentration may serve as n mold of 5x1018cm-3 here. As material gas for

introducing silicon, organic silanes, such as a silane or a tetraethyl silane, can be used. After such crystal growth, vacuum evaporationo formation is carried out so that the laminating of the metal used as an ohmic electrode, for example, the Ti (below)/aluminum/nickel/Au, (above) may be carried out as thickness of 25nm, 250nm, 40nm, and 45nm on aluminum0.3Ga0.7N layer 12, respectively, and it considers as the source electrode 18 and the drain electrode 19. Furthermore, among these, a work function is larger than titanium (Ti), and on aluminum0.3Ga0.7N layer 12, vacuum evaporationo formation is carried out and it considers as the gate electrode 20 so that the laminating of the combination of the metal which carries out the Schottky barrier to aluminum0.3Ga0.7N, for example, nickel (lower layer)/the Au, (upper layer) may be carried out as thickness of 50nm and 250nm, respectively. According to this example, the resistivity of an ohmic electrode was able to be reduced by forming the thin AlxGa(1-x) N layer 12 between the source drain electrodes 18 and 19 and the GaN layer 11. Moreover, in the structure of this example, since the thickness of the AlxGa(1-x) N layer 12 is limited to the narrow range, if the presentation of aluminum is decided, threshold voltage will serve as an almost fixed value. That is, desired threshold voltage can be obtained by changing the presentation ratio of aluminum.

(The 2nd example) Drawing 6 is a mimetic diagram showing the important section cross-section structure of the heterojunction field-effect transistor as the 2nd example of this invention. The same sign is given to the same element as what was mentioned above about drawing 1 thru/or drawing 5 about this drawing, and detailed explanation is omitted. In the case of the transistor of this example, like the conventional transistor, AlxGa(1-x) N layer 12A is thickly formed so that it may become desired threshold voltage. And it considers as the structure which carries out lamination of the lower 12B of the ohmic electrodes 18 and 19 to the range of 1nm - 6nm. Also in this structure, the same effectiveness as the 1st example is acquired. In order to create the structure of this example, on the occasion of the creation approach of the 1st example, the AlxGa(1-x) N layer 12 is thickly formed conventionally like structure, and before forming the source drain electrodes 18 and 19, the process which etches a part of AlxGa(1-x) N layer which forms these ohmic electrode is added. On the occasion of etching, it can carry out by the technique of reactive ion etching using chlorine gas etc. This structure can respond more flexibly in that desired threshold voltage is realized compared with the 1st example. However, the time amount and cost of creation increase at the point which needs to add the process of etching. About the electric-field structure transistor of this example, when contact resistance of the source electrode 18 and the drain electrode 19 was

measured, it has decreased to 1/10 of structures conventionally. Consequently, the fall and the transconductance of knee voltage of a drain current characteristic improved 20% 10%. Thereby, maximum of the frequency of 20GHz and the power addition effectiveness in AB class actuation was able to be conventionally enlarged 10% compared with structure.

(The 3rd example) Drawing 7 is a mimetic diagram showing the important section cross-section structure of the heterojunction field-effect transistor as the 3rd example of this invention. The same sign is given to the same element as what was mentioned above about drawing 1 thru/or drawing 6 also about this drawing, and detailed explanation is omitted. In the case of the transistor of this example, in the structure of the 2nd example, the field of etched AlxGa(1-x) N layer 12B is formed more widely than the source drain electrodes 18 and 19 used as an ohmic electrode. In the present process, it is required to give the allowances in consideration of "a doubling gap" to the mask used for etching of an AlxGa(1-x) N layer and the mask used for patterning of an ohmic electrode. Therefore, it is difficult to create correctly the structure expressed to drawing 6 , and the structure which prepared the margin like this example is easier for manufacture. Moreover, also in the transistor of this example, the resistivity of an ohmic electrode was able to be reduced by preparing thin AlxGa(1-x) N layer 12B between the source drain electrodes 18 and 19 and the GaN layer 11.

(The 4th example) Drawing 8 is a mimetic diagram showing the important section cross-section structure of the heterojunction field-effect transistor as the 4th example of this invention. The same sign is given to the same element as what was mentioned above about drawing 1 thru/or drawing 7 also about this drawing, and detailed explanation is omitted. In the case of the transistor of this example, in the structure of the 2nd example, the field of etched AlxGa(1-x) N layer 12B is formed more narrowly than the source drain electrodes 18 and 19 used as an ohmic electrode. Also in this example, since the margin in consideration of "a doubling gap" of the mask used for etching of an AlxGa(1-x) N layer and the mask used for patterning of an ohmic electrode is prepared as mentioned above about the 3rd example, manufacture is easy. Moreover, also in the transistor of this example, the resistivity of an ohmic electrode was able to be reduced by preparing thin AlxGa(1-x) N layer 12B between the source drain electrodes 18 and 19 and the GaN layer 11.

(The 5th example) Drawing 9 is a mimetic diagram showing the important section cross-section structure of the heterojunction field-effect transistor as the 5th example of this invention. Hereafter, the structure of the transistor of this example is

explained, referring to the production process. First, by approaches, such as the MOCVD method, on silicon on sapphire or a SiC substrate, it is thin, for example, 4nm of nucleation layers of AIN is formed, it is fully thick, for example, 2 micrometers of GaN layers 11 which serve as a channel on this are grown up, and 20nm, aluminum0.3Ga0.7N layer 13 [for example,], of AlxGa(1-x) N layers is grown up in order. The same gas as what was mentioned above about the 1st example can be used for the crystal growth by these MOCVD(s). Moreover, aluminum0.3Ga0.7N layer 13 is taken as the layer which contains silicon as an impurity so that the Donna concentration may serve as n mold of 5x1018cm-3. Suppose that the material gas for introducing Si is the same as that of the 1st example. Next, after making SiO2 film deposit with Heat CVD etc. all over a substrate, SiO2 mask is formed by performing wet etching and exfoliating a photoresist continuously with ammonium fluoride etc., performing patterning of a photoresist at a lithography process and using a photoresist as a mask. Inert gas, such as chlorine-based gas and an argon, was used, for example, n mold aluminum0.3Ga0.7N layer 13 is etched by ECR-RIBE (Electron Cyclotron Resonance-Reactive Ion BeamEtching). Next, ammonium fluoride etc. removes SiO2 mask, and it is with MBE (molecular-beam epitaxial) equipment etc., and is 1nm - 6nm. aluminum0.3Ga0.7N layer 12 from which it is the thickness of the range, for example, the mole ratio x of aluminum is set to 0.3 is re-grown up to be the whole surface. Next, after making SiO2 film deposit with Heat CVD etc. all over a substrate, patterning of a photoresist is performed at a lithography process. Ammonium fluoride etc. performs wet etching by using a photoresist as a mask. On aluminum0.3Ga0.7 N layer 12 which re-grew on the GaN layer 11 of the field where n mold aluminum0.3Ga0.7N layer 13 was removed by previous etching Ti (lower layer) / 25nm (upper layer) of each aluminum, and the laminated metal film that consists of 250nm are vapor-deposited with vacuum evaporationo equipment, after a lift-off process, heat treatment for [900 degrees-C] 30 seconds is performed for example, in nitrogen-gas-atmosphere mind, and the source electrode 18 and the drain electrode 19 are formed. Then, patterning of a photoresist is performed at a lithography process. Perform wet etching and with vacuum evaporationo equipment on aluminum0.3Ga0.7 N layer 12 which used the photoresist as the mask and re-grew on n mold aluminum0.3Ga0.7 N layer 13 continuously with ammonium fluoride etc. for example The laminated metal film which consists of nickel (lower layer) / 50nm (upper layer) of each Au, and 250nm is vapor-deposited, after a lift-off process, heat treatment for [300 degrees-C] 10 minutes is performed for example, in nitrogen-gas-atmosphere mind, and the gate electrode 20 is formed. According to this

example explained above, by forming the thick AlGaN layer 13, a gate part can control a threshold certainly and easily, and can acquire the contact resistance reduction effectiveness of this invention certainly by forming the thin AlGaN layer 12 in the contact section of a source drain electrode.

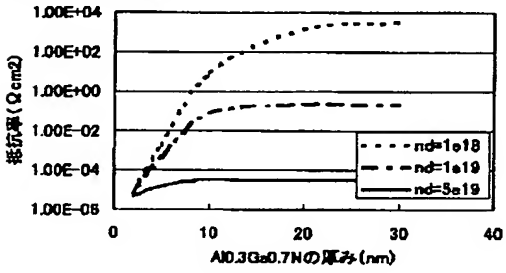
(The 6th example) Drawing 10 is a mimetic diagram showing the important section cross-section structure of the heterojunction field-effect transistor as the 6th example of this invention. Hereafter, the structure of the transistor of this example is explained, referring to the production process. First, are thin in the nucleation layer of AlN on silicon on sapphire or a SiC substrate by approaches, such as the MOCVD method. For example, are fully thick in the undoping GaN layer 11 which forms 4nm and serves as a channel on this. For example, 2 micrometers is grown up, undoping aluminum0.3Ga0.7N layer 12 which becomes a spacer layer on this is grown up by the thickness of the range of 1nm - 6nm, and n mold aluminum0.3Ga0.7N layer 16 [10nm] which becomes an electronic supply layer on this is grown up in order. Undoping aluminum0.3Ga0.7N layer 17 which besides becomes a shot key contact layer is formed in the thickness of 5nm. The same gas as what was mentioned above about the 1st example can be used for the crystal growth by these MOCVD(s). aluminum0.3Ga0.7N layer 16 which is an electronic supply layer is taken as the layer which contains silicon as an impurity so that the Donna concentration may serve as n mold of 5x1018cm-3. Suppose that it is the same as that of the 1st example also with the material gas for introducing silicon. Next, after making SiO2 film deposit with Heat CVD etc. all over a substrate, SiO2 mask is formed by performing wet etching and exfoliating a photoresist continuously with ammonium fluoride etc., performing patterning of a photoresist at a lithography process and using a photoresist as a mask. For example, n mold aluminum0.3Ga0.7N layer 16 using inert gas, such as chlorine-based gas and an argon, which is an electronic supply layer, and undoping aluminum0.3Ga0.7N layer 17 which are a shot key contact layer are etched by ECR-RIBE. Next, after making SiO2 film deposit with Heat CVD etc. all over a substrate, patterning of a photoresist is performed at a lithography process. Ammonium fluoride etc. performs wet etching by using a photoresist as a mask. To then, up to undoping aluminum0.3Ga0.7 N layer 12 which is the spacer layer exposed to the front face by previous etching Ti (lower layer) / 25nm (upper layer) of each aluminum, and the laminated metal film that consists of 250nm are vapor-deposited with vacuum evaporationo equipment, after a lift-off process, heat treatment for [900 degrees-C] 30 seconds is performed for example, in nitrogen-gas-atmosphere mind, and the source electrode 18 and the drain electrode 19 are formed. then, a lithography

process -- patterning of a photoresist -- carrying out -- a photoresist -- a mask -- carrying out -- ammonium fluoride etc. -- wet etching -- carrying out -- continuing -- vacuum evaporationo equipment -- for example, nickel (lower layer)/Au (upper layer) -- the laminated metal film which consists of 50nm and 250nm, respectively -- vapor-depositing -- after a lift-off process -- for example, the inside of nitrogen-gas-atmosphere mind -- heat treatment for [300 degrees-C] 10 minutes -- carrying out -- an undoping aluminum0.3Ga0.7N layer -- the gate electrode 20 is formed in up to 17. Also in this example, the resistivity of an ohmic electrode was able to be reduced by forming the thin AlxGa(1-x) N layer 12 between the source drain electrodes 18 and 19 and the GaN layer 11. In the above, the gestalt of operation of this invention was explained, illustrating an example. However, this invention is not limited to each example mentioned above. For example, this invention is not limited to the transistor with which it expressed as an example, in addition in addition to this, it can apply to light emitting diode, semiconductor laser, or various kinds of semiconductor devices, the same effectiveness can be acquired, and these are also included by the range of this invention. Moreover, all the semiconductor devices obtained by carrying out a design change, not being limited to what was expressed as an example, in addition this contractor applying this invention also about the structure of a transistor are included by the range of this invention. For example, that in which this contractor did the design change suitably about the ingredient which constitutes each part of a semiconductor device, an addition impurity, thickness, the configuration, the conductivity type, the formation approach, etc. is included by the range of this invention.

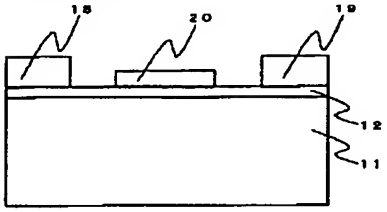
[Effect of the Invention] as explained in full detail above, according to this invention, it becomes possible to lower more sharply than before the contact resistance to the electron of the semiconductor device using a nitride semi-conductor -- for example Since the current to which the electron of the hetero interface produced according to polarization peculiar to a nitride semi-conductor hetero interface originated in tunneling by making an AlxGa(1-x) N layer thin in the case of the field-effect transistor is increased, the low ohmic electrode of contact resistance can be formed. As the result, the knee voltage of a drain current characteristic is low, and can make a transconductance high, and the actuation of high power, efficient, and a RF of it is attained. That is, according to this invention, the merit on industry is great at the point that it becomes possible to form certainly and easily the ohmic contact by the side of n of a nitride semiconductor device, and the property of various kinds of semiconductor devices can be improved.

DRAWINGS

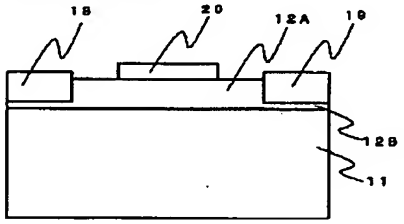
[Drawing 4]



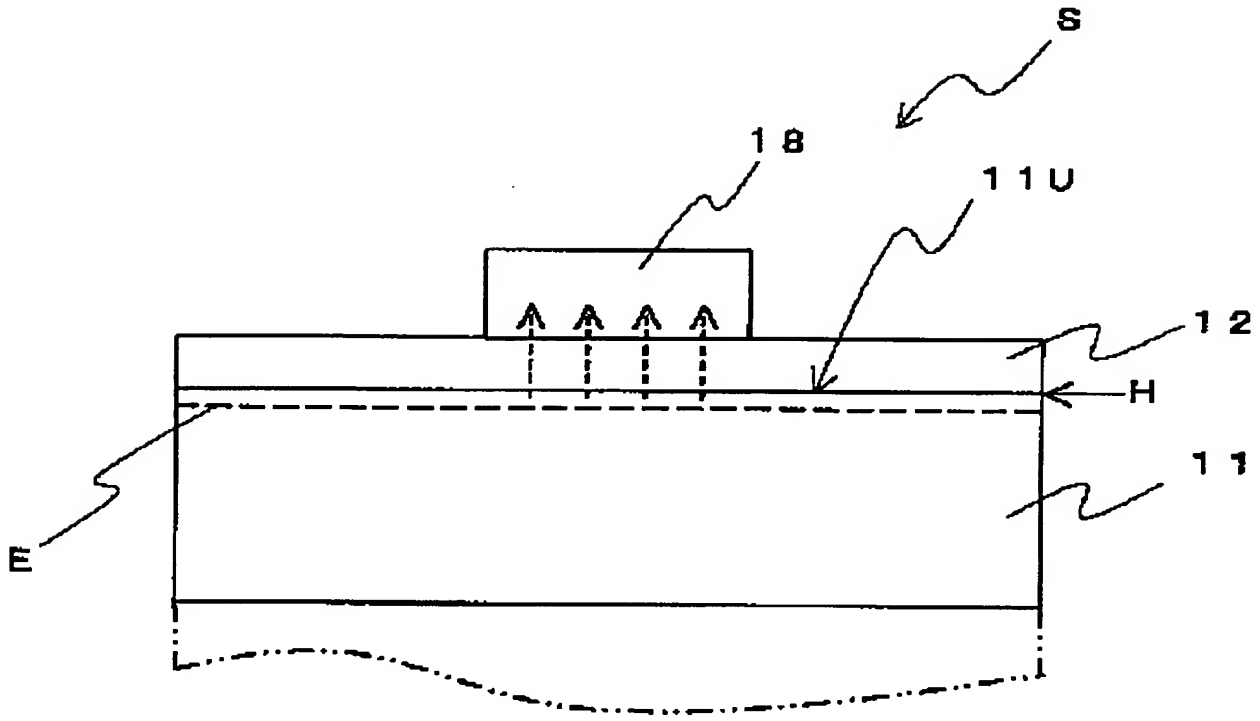
[Drawing 5]



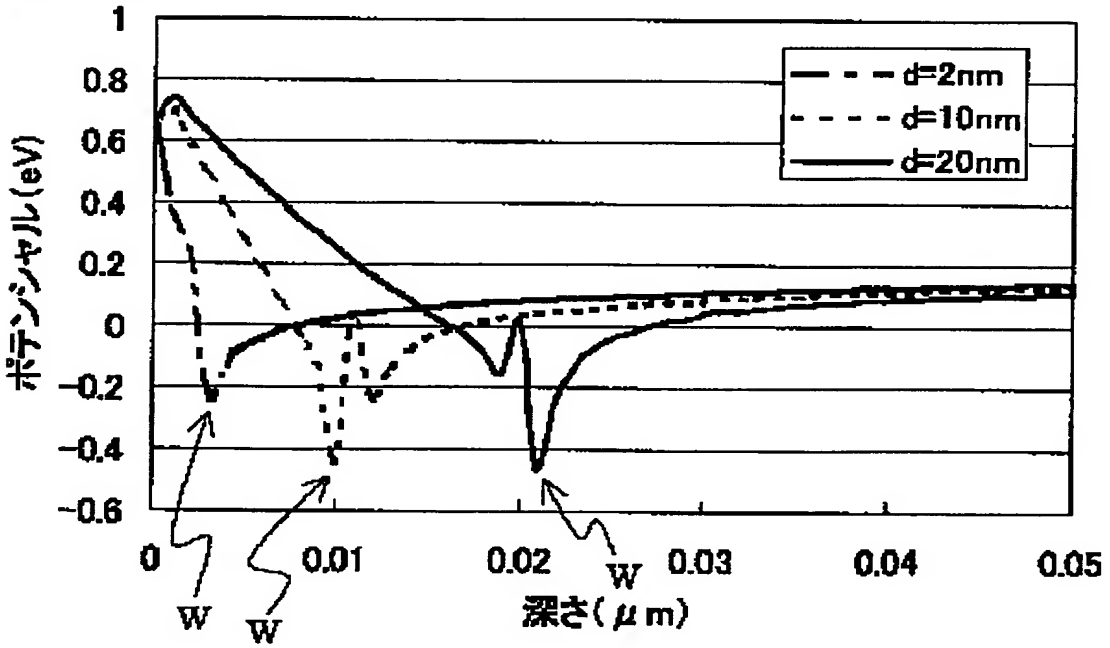
[Drawing 6]



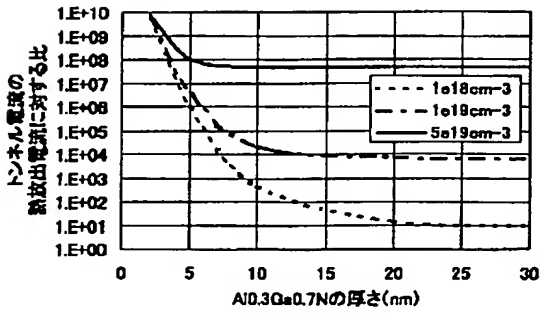
[Drawing 1]



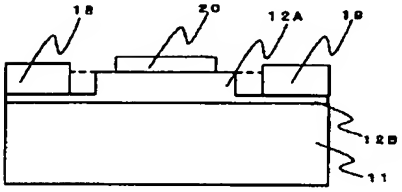
[Drawing 2]



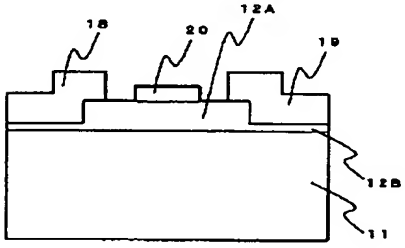
[Drawing 3]



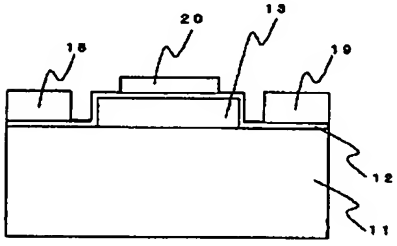
[Drawing 7]



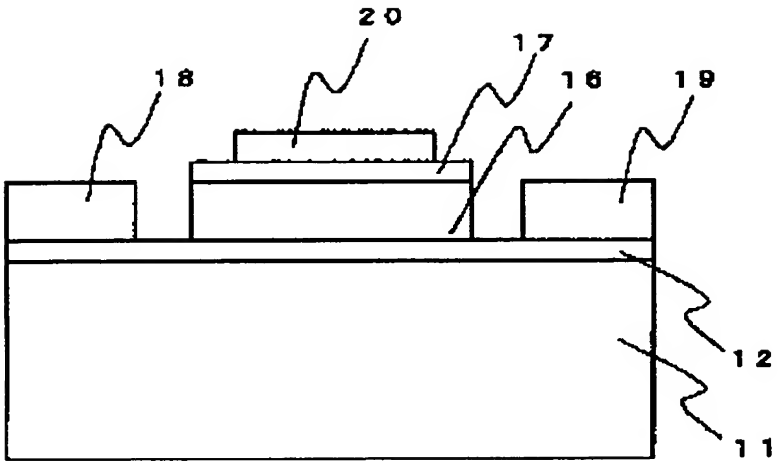
[Drawing 8]



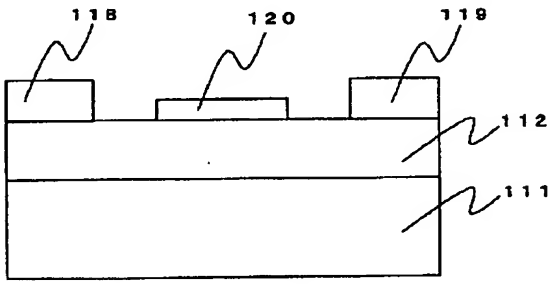
[Drawing 9]



[Drawing 10]



[Drawing 11]



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